CIRCUIT TECHNIQUES FOR EFFICIENT LINEARISED GaAs MMIC's

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Abstract: This paper is concerned with novel circuit designs for monolithic microwave integrated circuit technology using depletion-mode GaAs MESFET's. A synthesis method leading to high efficiency implementation of linear functions based on a square-law FET characteristic is presented and used to design a linearised isolator which is compared with a non-linearised design. A circuit equivalent to a common-gate FET, but with linearity, high efficiency, and reduced FET gate-width and power consumption, is proposed for future use in improved isolators and amplifiers.

1 INTRODUCTION

Many system functions realised by traditional microwave tecnologies are now being tackled using GaAs monolithic microwave integrated circuit (MMIC) design techniques in order to reduce cost, size and weight and provide additional performance functions [1]. The new techniques discussed in this paper are aimed at achieving high power-efficiency and linearity, and also minimum total FET gate-width, in order to minimise power consumption, dissipation and die size. In view of its simplicity and inspiring recent work [2], the isolator is used as a test vehicle to explore the new techniques.

2 ISOLATOR IMPLEMENTATION

The isolator is a 2-port network required to have a forward gain of unity, reverse gain of zero and perfect matching at both ports, or, in terms of **S** and **Y** parameters,

$$\underline{S}_{iso}=\begin{bmatrix}0 & 0\\ 1 & 0\end{bmatrix} \quad \underline{Y}_{iso}=\begin{bmatrix}G_o & 0\\ -2G_o & G_o\end{bmatrix} \quad \text{... (1)}$$

where G_o is 20 mS assuming a 50 Ω environment. We now consider implementation of (1) using depletion-mode GaAs MESFET's which can be described by

$$I_d=\beta\left(V_{gs}-V_T\right)^2 \quad \text{... (2)}$$

$$I_s=-I_d \quad \text{... (3)}$$

where I_d and I_s are drain and source current, V_{gs} is gate-source voltage and β and V_T are constants. For small signals, we may linearise (2) and represent the FET by

$$\begin{bmatrix}i_g\\ i_s\\ i_d\end{bmatrix}=\begin{bmatrix}0 & 0 & 0\\ -G_m & G_m & 0\\ G_m & -G_m & 0\end{bmatrix}\begin{bmatrix}v_g\\ v_s\\ v_d\end{bmatrix} \quad \text{... (4)}$$

where G_m is small-signal transconductance ($=i_d/v_{gs}=dI_d/dV_{gs}$). From (4) the common-gate FET and common-drain FET may be described by

$$\underline{Y}_{cg}=\begin{bmatrix}G_m & 0\\ -G_m & 0\end{bmatrix} \quad \underline{Y}_{cd}=\begin{bmatrix}0 & 0\\ -G_m & G_m\end{bmatrix} \quad \text{... (5)}$$

Hence the isolator function in (1) may be realised by a parallel connection of a common-gate and common-drain FET where for both FET's $G_m = G_o$. Although this realisation is attractive because it is economical, the FET characteristic in (2) implies non-linearity unless signal levels are kept very small. Such non-linearity can be reduced by using balanced systems [2]. Considering the requirement to maintain accurately balanced signals in such a system and the doubling in total FET gate-width, we now consider an alternative approach of direct synthesis of linear functions [3].

3 SYNTHESIS OF LINEARISED FUNCTIONS

Using the simple FET model of (2), we form the system current [3] as a sum of m positively-weighted and n negatively-weighted FET drain currents where for each FET, V_{gs} is a weighted sum of system input voltages V_1 V_2 ... V_p with weighting factors a_{ik} and b_{jk} restricted to -1, 0 or +1

$$I=\sum_{i=1}^{m}\beta\left(\sum_{k=1}^{p}a_{ik}V_k-V_T\right)^2-\sum_{j=1}^{n}\beta\left(\sum_{k=1}^{p}b_{jk}V_k-V_T\right)^2 \quad \text{... (6)}$$

Terms proportional to V_T^2 are eliminated by letting n=m [3].

We now define m x p matrices **A** and **B** comprising weighting factors a_{ik} and b_{jk}, the p x 1 column vector of input voltages $\underline{v}$ = (V_1 V_2 ... V_k ... V_p)^t and an m x 1 column vector of constants $\underline{V_T}$ = V_T(1 1 ... 1)^t. Eqn (2) is equivalent to [4]

$$I=\beta\left\{\underline{v}^t\left(A^tA-B^tB\right)\underline{v}+2\underline{v_T}^t(B-A)\underline{v}\right\} \quad \text{... (7)}$$

The condition that input voltage-squared terms vanish is that

$$A^tA-B^tB=\begin{bmatrix}0 & \cdot & \cdot & \cdot\\ \cdot & 0 & \cdot & \cdot\\ \cdot & \cdot & \cdot & \cdot\\ \cdot & \cdot & \cdot & 0\end{bmatrix} \quad \text{or} \quad \sum_{i=1}^{m}a_{ik}{}^2=\sum_{i=1}^{m}b_{ik}{}^2 \quad \text{for all k = 1 ...p} \quad \text{... (8)}$$

or each column of **A** must contain the same number of zeros as the corresponding column of **B**.

The coefficient matrices **A** and **B** may be chosen to yield a wide range of conductance and multiplier functions [3] and

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Table 1: Conductance/multiplier function examples

	A	B	I
Multiplier	$\begin{bmatrix}1 & 0\\ 0 & -1\end{bmatrix}$	$\begin{bmatrix}1 & -1\\ 0 & 0\end{bmatrix}$	$2\beta V_1 V_2$
Conductance	$[-1 \quad 1]$	$[1 \quad 1]$	$4\beta V_1(V_T-V_2)$

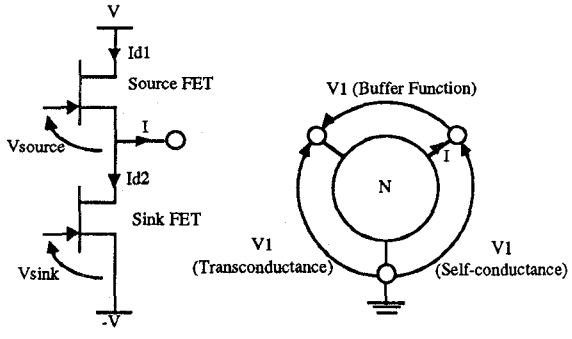

Fig 1: Architecture

Fig 2: Configurations

two examples are given in Table 1. For the conductance function, m is unity implying that the current is synthesised in (6) as the difference in the drain currents of two MESFET's and a circuit architecture is shown in Fig 1. From **A** and **B** in Table 1, the gate-source voltage of the source and sink MESFET, are required to be

$$V_{source} = -V_1 + V_2 \qquad V_{sink} = V_1 + V_2 \quad \ldots (9)$$

We interpret V_2, in accordance with [5], as the source and sink MESFET quiescant gate-source voltage, which can be used to tune the transconductance with respect to the signal input voltage V_1, according to the expression in Table 1.

It has been shown [5] that, in order to maximise output current and provide a high power conversion efficiency of

$$\eta_c = \frac{2}{3}\left(\hat{V}_L / V\right) \quad \ldots (10)$$

where V is power supply voltage and $\hat{V}_L$ is peak output voltage, the quiescant gate-source voltage of the source and sink MESFET should be

$$V_2 = \frac{1}{2}(V_{\max} + V_T) \quad \ldots (11)$$

where V_{max} is the maximum limit on FET gate-source voltage to avoid forward biassing the gate-channel Schottky diode. The architecture in Fig 1 identifies a node at which the linearised current function I is realised. The signal input voltage V_1 may be defined with respect to this node, ground and a third node as shown in Fig 2, thus defining three different configurations, transconductance, self-conductance and buffer function, which may be thought of as linearised equivalents of the common-source, common-gate and common-drain FET, respectively [4,6].

4 LINEARISED ISOLATOR

A linearised isolator has been designed and submitted for fabrication. It is based on a decomposition of the isolator **Y** matrix of (1) into the sum of three components

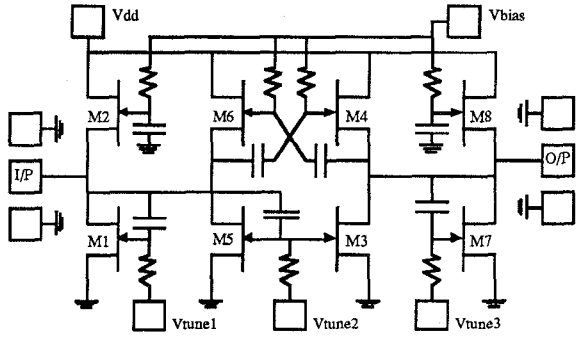

Fig 3: Circuit Diagram of Isolator 1

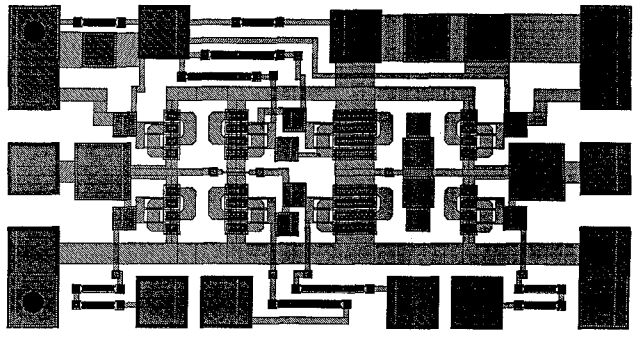

Fig 4: Layout plot of MMIC isolator

$$\underline{Y}_{iso} = \begin{bmatrix}G_o & 0\\ 0 & 0\end{bmatrix} + \begin{bmatrix}0 & 0\\ -2G_o & 0\end{bmatrix} + \begin{bmatrix}0 & 0\\ 0 & G_o\end{bmatrix} \quad \ldots (12)$$

which are a self-conductance G_o at port 1, a transconductance $2G_o$ linking port 1 to port 2 and a self-conductance G_o at port 2, respectively.

The basic circuit diagram of the isolator is shown in Fig 3, which uses previously reported circuit blocks [5]. M1/M2 and M7/M8 (and associated CR-networks) form the two self-conductance circuits and M3-M6 form the transconductance. M1, M3 and M7 are the sink FET's; M2, M4 and M8 are the source FET's. The bias/tuning voltage V_2 for each block is supplied via the terminals $V_{tune1,\ 2,\ 3}$. For the self-conductances, the CR-networks are sufficient to provide the source and sink FET gate-source voltages according to (9). For the transconductance, MESFET's M5/M6 and associated CR-networks invert the input voltage to $-V_1$ before applying it to the gate-source port of source MESFET M4 [5,7].

The circuit is designed for implementation using the Plessey process [8]. The layout shown in Fig 4 includes coupling capacitors between the three sections which are not strictly necessary. Power supply voltage is 6 V and quiescant power consumption 250 mW; chip area is 1.5 mm x 0.75 mm.

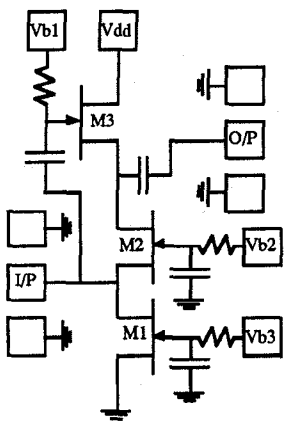

Fig 5: Circuit of Isolator 2

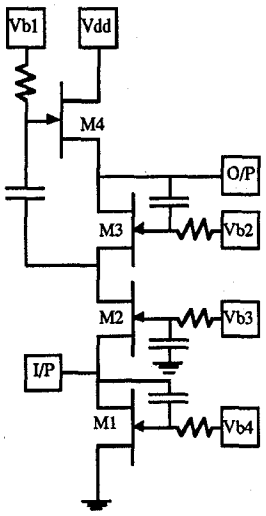

Fig 10: Novel Circuit

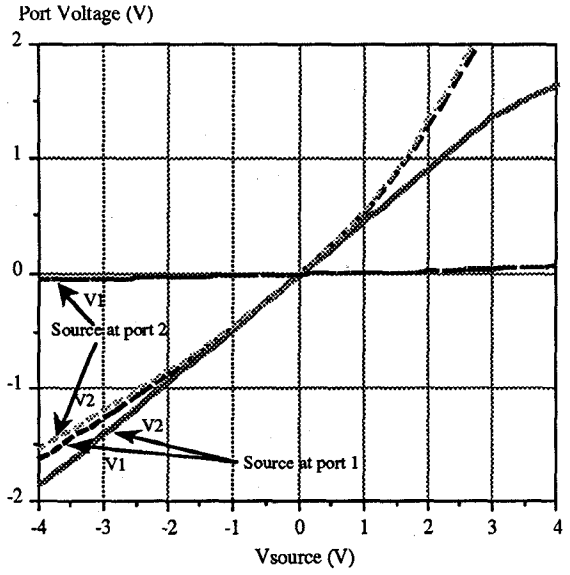

Fig 6: Simulated Linearity of Isolator 2

5 SIMULATED ISOLATOR PERFORMANCE

We now compare the simulated performance of isolator 1 in Fig 3 with the circuit in Fig 5 which consists of a parallel combination of a common-gate FET (M2) with a common-drain FET (M3) as discussed in section 2; M1 realises a constant current source to satisfy DC conditions. Although the number of FET's in Fig 5 is much less than in Fig 3, the gate-widths must be considered; in Fig 5, the width W of the FET's must provide a small-signal transconductance (G_m in (5)) of 20 mS; by virtue of the pushpull linearisation, M1, M2, M7 and M8 in Fig 3 have width W/2, M3 and M4 have width W (to realise the 2Go term in (12)), and the widths of M5 and M6 are arbitrary and may be W/2. Thus the cost in terms of total gate-width of the linearised circuit in Fig 3 is an increase of 66%, but future work will reduce and even reverse this.

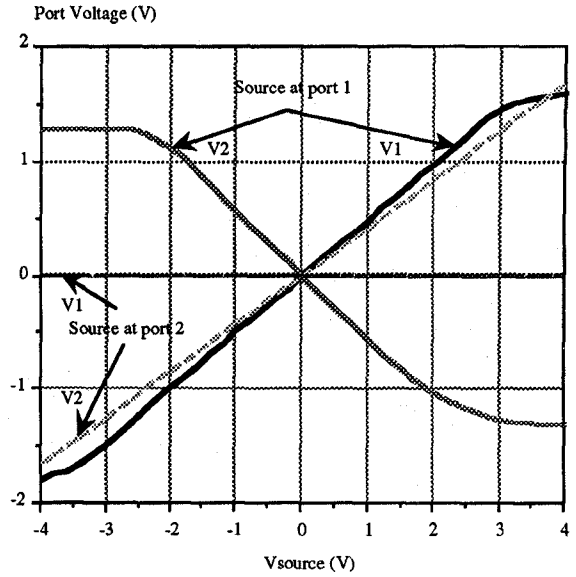

Fig 7: Simulated Linearity of Isolator 1

Two forms of SPICE simulation are presented. Figs 6 and 7 are intended to indicate nonlinear behaviour and show the port voltages (V1 and V2) for a ramped 50 Ω source at port 1 and at port 2. Figs 8 and 9 show small-signal S-parameters as a function of frequency. The non-linearity of both ports of isolator 2, expected from the FET characteristic of (2), is clearly shown in Fig 6 (V1 - source at port 1 and V2 source at port 2). An unexpected result is the linearity of the forward transfer characteristic in Fig 6 (V2 - source at port 1) which can be shown to be due to approximate cancellation of the input and output port non-linearities. It is intended to study this form of approximate linearisation in more detail and attempt to apply it generally. Fig 7 for the linearised circuit exhibits good linearity at both ports; linearity of the forward transfer characteristic can be improved by optimum choice of power supply voltage and biassing in relation to FET parameters; these factors are more critical for a linearised circuit.

The small-signal curves in Figs 8 and 9 confirm improved isolation for the linearised isolator 1 but a reduction in bandwidth attributed to the loading of the input port by the input capacitance of the $2G_o$ transconductance stage; this is an architectural feature which will be overcome in future work. Deterioration in S22 in Fig 8 and S11 and S22 in Fig 9 at low frequencies is due to coupling capacitors included in the design; they will be removed in future designs in which case curves similar to S11 in Fig 8 are obtained.

6 NOVEL LINEARISED CIRCUIT

In view of the disadvantages of the isolator architecture chosen based on the decomposition of (12), other forms of linearised circuit are being investigated. One possibility is to implement the sum of **Y** matrices in (5) but using linearised circuits. $\mathbf{Y}_{cd}$ can be realised by the linearised buffer circuit in [4] which is based on the linearisation in section 3 and offers a 25% saving in total gate-width compared with the regular common-drain FET arrangement. For realising $\mathbf{Y}_{cg}$ we propose the new circuit in Fig 10 (adjacent Fig 5) which can be regarded as a linearised version of a common-gate FET.

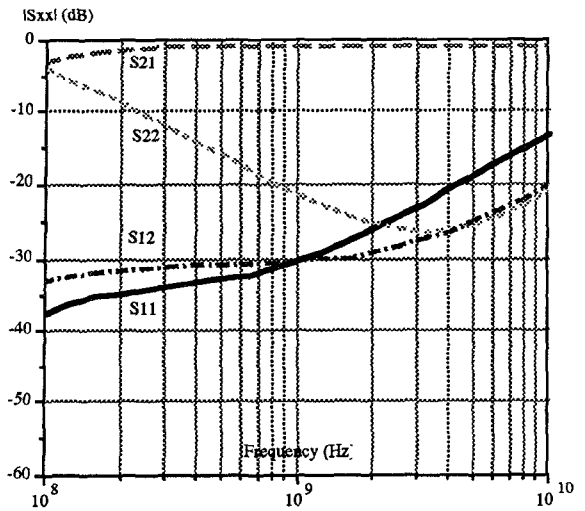

Fig 8: Simulated S-parameters of Isolator 2

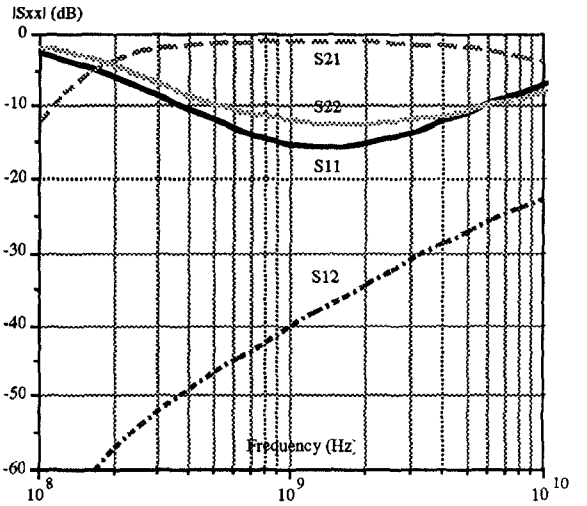

Fig 9: Simulated S-parameters of Isolator 1

M2 and M1 are the source and sink FET's for the input port. If input voltage is V_1 and quiescant FET gate-source voltage V_2 ($\equiv V_{b4}$) then M2 and M1 gate-source voltages are as in (9). For the output port, M4 and M3 are the source and sink FET's. For MESFET's M4 and M3, the gate-source voltages are reversed in relation to (9) [4]. Thus the output current equals the input current as required.

Compared with the common-gate FET with current sources at source and drain, the circuit in Fig 10 offers a 33% reduction in total gate-width and yet is linearised and has high efficiency according to (10). Should not linearised circuits be the natural first choice of the circuit designer?

7 CONCLUSIONS

We have presented an existence proof of an MMIC isolator circuit which is linearised in terms of its port and transfer characteristics. When realistic MESFET models are used in simulation [9], linearisation is not perfect, but it has been shown that slight changes in the widths of the FET's can yield excellent linearity [4]. This aspect of the work is being actively pursued as well as study of 3rd harmonic due to finite FET drain-source conductance and ways of reducing or cancelling this effect. We have also presented here a novel linearised version of the common-gate FET, which is economical in terms of total FET gate-width and which could form the basis of future efficient linearised isolator circuits. It is hoped that the techniques being developed for isolators will pave the way toward new architectures for linearised amplifiers where the input and output port impedeances are synthesised along with the transmission function, as well as attractive implementations of other functions such as the multiplier in Table 1.

ACKNOWLEDGEMENTS

The author would like to thank the following: Carlos Losada Sean Smedley and Ahmad Khanifar of University College, Mahmood Darvishzadeh of SERC Rutherford Appleton Labs and Chris Toumazou of Imperial College.

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